AMENDMENT TO THE CLAIMS[1]

1-29. (previously cancelled)

30. (previously added) A method of etching a semiconductor wafer comprising a silicon oxide layer formed over a silicon nitride layer, the method comprising plasma etching the silicon oxide layer in an etchant environment comprising a fluorohydrocarbon, wherein the fluorohydrocarbon contains at least as many hydrogen atoms as fluorine atoms, and wherein the etchant environment provides silicon oxide-to-silicon nitride selectivity.

31. (previously added) The method of claim 30, wherein the fluorohydrocarbon is CH_3F.

32. (previously added) The method of claim 30, wherein the fluorohydrocarbon contains the same number of hydrogen and fluorine atoms.

33. (previously added) The method of claim 32, wherein the fluorohydrocarbon is CH_2F_2.

34. (previously added) The method of claim 30, wherein the etchant environment further comprises a fluorinated gas.

35. (previously added) The method of claim 34, wherein the fluorinated gas is selected from the group consisting of CF_4 and CHF_3.

36. (previously added) The method of claim 34, wherein the etchant environment further comprises an inert gas.

37. (previously added) The method of claim 36, wherein the inert gas is argon.

38. (previously added) The method of claim 30, wherein the silicon oxide layer is formed directly above the silicon nitride layer.

39. (previously added) The method of claim 30, wherein the silicon oxide is selected from the group consisting of undoped silicon oxide and doped silicon oxide.

40. (previously added) The method of claim 30, wherein the silicon nitride layer is formed with an uneven topography.

41. (previously added; currently amended) The method of claim 30, wherein the semiconductor wafer further comprises two [polysilicon] conductors, wherein the silicon nitride

---

[1] Claims noted as "previously added" were added earlier by preliminary amendment. Applicant has noticed that these claims were referred to in earlier papers as "original," but this is believed inaccurate given that the claims were entered upon preliminary amendment.

layer is formed above the [polysilicon] conductors, and wherein the plasma etching forms an opening in the silicon oxide between the [polysilicon] conductors.

42. (previously added) The method of claim 30, further comprising heating the semiconductor wafer during plasma etching.

43. (previously added) The method of claim 42, wherein the semiconductor wafer is heated to between about 20 and 80 degrees C.

44. (previously added) The method of claim 42, wherein the semiconductor wafer is heated to between about 30 and 60 degrees C.

45. (previously added) The method of claim 42, wherein the semiconductor wafer is heated to between about 35 and 50 degrees C.

46. (previously added) The method of claim 42, wherein the semiconductor wafer is heated by heating an electrode adjacent to the semiconductor wafer.

47. (previously added) The method of claim 46, wherein the electrode is heated to between about 20 and 80 degrees C.

48. (previously added) The method of claim 46, wherein the electrode is heated to between about 30 and 60 degrees C.

49. (previously added) The method of claim 46, wherein the electrode is heated to between about 35 and 50 degrees C.

50-59. (canceled)

60. (previously added) The method of claim 30, wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 10-to-1.

61. (previously added) The method of claim 30, wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 20-to-1.

62. (previously added) The method of claim 30, wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 30-to-1.

63. (previously added) A method of etching a semiconductor wafer comprising a silicon oxide layer formed over a silicon nitride layer, the method comprising plasma etching the semiconductor wafer in an etchant environment, wherein the method comprises heating the semiconductor wafer during plasma etching to increase the silicon oxide-to-silicon nitride selectivity.

64. (previously added) The method of claim 63, wherein the etchant environment comprises a fluorohydrocarbon, wherein the fluorohydrocarbon contains at least as many hydrogen atoms as fluorine atoms.

65. (previously added) The method of claim 64, wherein the fluorohydrocarbon is CH_3F.

66. (previously added; previously amended) The method of claim 63, wherein the etchant environment comprises a fluorohydrocarbon, wherein the fluorohydrocarbon contains the same number of hydrogen and fluorine atoms.

67. (previously added) The method of claim 66, wherein the fluorohydrocarbon is CH_2F_2.

68. (previously added) The method of claim 63, wherein the etchant environment further comprises a fluorinated gas.

69. (previously added) The method of claim 68, wherein the fluorinated gas is selected from the group consisting of CF_4 and CHF_3.

70. (previously added) The method of claim 68, wherein the etchant environment further contains an inert gas.

71. (previously added) The method of claim 70, wherein the inert gas is argon.

72. (previously added) The method of claim 63, wherein the semiconductor wafer is heated to between about 20 and 80 degrees C.

73. (previously added) The method of claim 63, wherein the semiconductor wafer is heated to between about 30 and 60 degrees C.

74. (previously added) The method of claim 63, wherein the semiconductor wafer is heated to between about 35 and 50 degrees C.

75. (previously added) The method of claim 63, wherein the semiconductor wafer is heated by heating an electrode adjacent to the semiconductor wafer.

76. (previously added) The method of claim 75, wherein the electrode is heated to between about 20 and 80 degrees C.

77. (previously added) The method of claim 75, wherein the electrode is heated to between about 30 and 60 degrees C.

78. (previously added) The method of claim 75, wherein the electrode is heated to between about 35 and 50 degrees C.

79-88. (canceled)

89. (previously added) The method of claim 63, wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 10-to-1.

90. (previously added) The method of claim 63, wherein the silicon oxide-to-silicon nitride selectivity is greater than 20-1.

91. (previously added) The method of claim 63, wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 30-to-1.

92. (previously added) The method of claim 63, wherein the silicon oxide layer is formed directly above the silicon nitride layer.

93. (previously added) The method of claim 63, wherein the silicon oxide is selected from the group consisting of undoped silicon oxide and doped silicon oxide.

94. (previously added) The method of claim 63, wherein the silicon nitride layer is formed with an uneven topography.

95. (previously added; currently amended) The method of claim 63, wherein the semiconductor wafer further comprises two [polysilicon] conductors, wherein the silicon nitride layer is formed above the [polysilicon] conductors, and wherein the plasma etching forms an opening in the silicon oxide between the [polysilicon] conductors.

96. (previously added) A method of etching a semiconductor wafer containing a silicon oxide layer formed over a silicon nitride layer, the method comprising plasma etching the semiconductor wafer using an etch environment that provides a silicon oxide-to-silicon nitride selectivity of greater than or equal to 10-to-1.

97. (previously added) The method of claim 96, wherein the etch environment comprises a first gas selected from the group comprising CH_3F and CH_2F_2.

98. (previously added) The method of claim 97, wherein the etch environment further comprises a second fluorinated gas.

99. (previously added) The method of claim 98, wherein the second fluorinated gas is selected from the group consisting of CF_4 and CHF_3.

100. (previously added) The method of claim 98, wherein the etch environment further comprises an inert gas.

101. (previously added) The method of claim 100, wherein the inert gas is argon.

102. (previously added) The method of claim 96, further comprising heating the semiconductor wafer during plasma etching.

103. (previously added; currently amended) The method of claim 102, [wherein the method is performed within an etch chamber comprising a wafer chuck for holding the semiconductor wafer and an etch chamber side wall, and wherein heating the semiconductor wafer involves heating the wafer chuck] wherein the semiconductor wafer is heated to between about 20 and 80 degrees C.

104. (previously added; currently amended) The method of claim [103] 102, [wherein the wafer chuck is heated to at least about 30 degrees Celsius] wherein the semiconductor wafer is heated to between about 30 and 60 degrees C.

105. (previously added; currently amended) The method of claim [103] 102, [wherein the wafer chuck is heated to from about 30 to about 100 degrees Celsius] wherein the semiconductor wafer is heated to between about 35 and 50 degrees C.

106. (previously added; currently amended) The method of claim 102, [wherein the method is performed within an etch chamber comprising a wafer chuck for holding the semiconductor wafer and an etch chamber side wall, and wherein heating the semiconductor wafer involves heating the etch chamber side wall] wherein the semiconductor wafer is heated by heating an electrode adjacent to the semiconductor wafer.

107. (previously added; currently amended) The method of claim 106, [wherein the side wall is heated to at least about 50 degrees Celsius] wherein the electrode is heated to between about 20 and 80 degrees C.

108. (previously added; currently amended) The method of claim 106, [wherein the side wall is heated to from about 50 to 100 degrees Celsius] wherein the electrode is heated to between about 30 and 60 degrees C.

109. (previously added; currently amended) The method of claim [102] 106, [wherein the method is performed within an etch chamber comprising a wafer chuck for holding the semiconductor wafer and an etch chamber side wall, and wherein heating the semiconductor wafer involves heating the wafer chuck and heating the etch chamber side wall] wherein the electrode is heated to between about 35 and 50 degrees C.

110. (previously added; currently amended) The method of claim [109] 97, [wherein the wafer chuck is heated to at least about 30 degrees Celsius, and wherein the side wall is heated to at least about 50 degrees Celsius] wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 20-to-1.

111. (previously added; currently amended) The method of claim [109] 97, [wherein the wafer chuck is heated to from about 30 to about 100 degrees Celsius] wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 30-to-1.

112. (previously added; currently amended) The method of claim [109] 97, [wherein the side wall is heated to from about 50 to 100 degrees Celsius] wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 50-to-1.

113. (previously added; currently amended) The method of claim [112] 102, [wherein the silicon dioxide-to-silicon nitride selectivity is greater than or equal to 10-to-1 but less than or equal to 33-to-1] wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 20-to-1.

114. (previously added; currently amended) The method of claim [113] 102, [wherein the silicon dioxide-to-silicon nitride selectivity is greater than or equal to 10-to-1 but less than or equal to 50-to-1] wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 30-to-1.

115. (previously added; currently amended) The method of claim 96, wherein the silicon [di]oxide-to-silicon nitride selectivity is greater than or equal to 20-to-1.

116-117. (canceled)

118. (previously added; currently amended) The method of claim 96, wherein the silicon [di]oxide-to-silicon nitride selectivity is greater than or equal to 30-to-1.

119. (previously added; currently amended) The method of claim [118] 96, wherein the silicon [di]oxide-to-silicon nitride selectivity is greater than or equal to [30-to-1 but less than or equal to] 50-to-1.

120. (previously added) The method of claim 96, wherein the silicon oxide layer is formed directly above the silicon nitride layer.

121. (previously added) The method of claim 96, wherein the silicon oxide is selected from the group consisting of undoped silicon oxide and doped silicon oxide.

122. (previously added) The method of claim 96, wherein the silicon nitride layer is formed with an uneven topography.

123. (previously added; currently amended) The method of claim 96, wherein the semiconductor wafer further comprises two [polysilicon] conductors, wherein the silicon nitride layer is formed above the [polysilicon] conductors, and wherein the plasma etching forms an opening in the silicon oxide between the [polysilicon] conductors.

124. (new) The method of claim 41, wherein the conductors are comprised of polysilicon.

125. (new) The method of claim 95, wherein the conductors are comprised of polysilicon.

126. (new) The method of claim 123, wherein the conductors are comprised of polysilicon.